

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

7-13-05

Title of Invention

Method and apparatus for specifying encoded sub-networks

Application Number : 10/066188
Confirmation Number: 4299
First Named Applicant: Steven Teig
Attorney Docket Number: SPLX.P0095
Art Unit: 2825
Examiner: Sun J. Lin
Search string: (6587990 or 6594808 or 5493504 or 66873883).pn



US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
JAL	1	6587990	2003-07-01	Andreev et al.		—	—
JAL	2	6594808	2003-07-15	Kale et al.	B1	—	—
JAL	3	5493504	1996-02-20	Minato		—	—
JAL	4	66873883	2004-02-03	Cohn et al.	B2	—	—

Signature

Examiner Name	Date
James Sun & Co	9-1-05

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

6-24-05

Title of Invention

Method and Apparatus for Specifying Encoded Sun-Networks

Application Number : 10/066188



Confirmation Number: 4299

First Named Applicant: Steven Teig

Attorney Docket Number: SPLX.P0095

Art Unit: 2825

Examiner: ~~Kenny Lin~~ LIN, SUN JAMES

Search string: (6140839 or 20020079921).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
Jes	1	6140839	2000-10-31	Kaviani		—	—

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
Jes	1	20020079921	2002-06-27	Kaviani		—	—

Signature

Examiner Name	Date
James Sun Bin	9-1-05

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3-23-05

Title of Invention

Method and apparatus for specifying encoded sub-networks

Application Number : 10/066188
Confirmation Number: 4299
First Named Applicant: Steven Teig
Attorney Docket Number: SPLX.P0095 (2002-106)
Art Unit: ~~2154~~ 2825
Examiner: ~~KENNY SLIN~~ LIN, SUN JAMES
Search string: (6333918).pn



US Patent Documents

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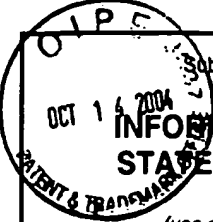
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
<i>JA</i>	1	6333918	2001-12-25	Hummel	B1	—	—

Signature

Examiner Name	Date
<i>James Sun</i>	3-1-05

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 <p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p>(use as many sheets as necessary)</p>				Application Number	10/066,188
				Filing Date	1/31/2002
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2402 2825
				Examiner Name	Eron L. Serrell <i>LIN, SUN JAMES</i>
Sheet	1	of	1	Attorney Docket Number	SPLX.P0095

NON PATENT LITERATURE DOCUMENTS			
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>JS</i>	1.	DREESEN J., Standard Cell Development Flow, IEEE, 1990, pp. 450-455	

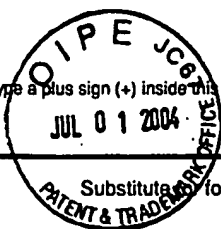
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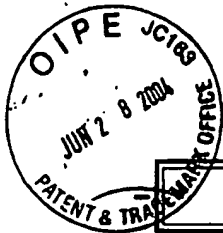
NON PATENT LITERATURE DOCUMENTS			
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gsl	1.	Krishnamoorthy et al., Boolean Matching of Sequential Elements, Proceedings of the 31st annual conference on Design automation conference, pp. 691-697, June 06-10, 1994, San Diego, California, United States.	

Examiner Signature	<i>James Sun</i>	Date Considered	9-1-05
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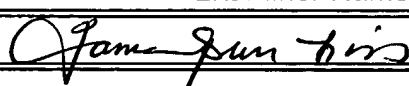
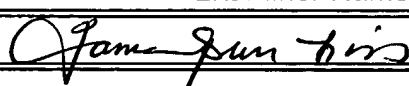
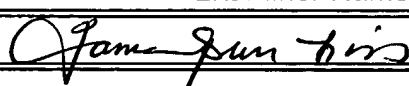
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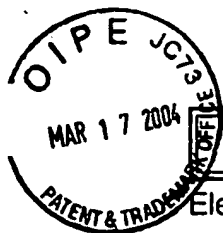


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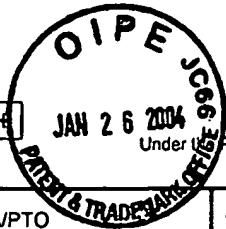


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				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2661 2825
				Examiner Name	LIN, SUN JAMES
Sheet	1	of	1	Attorney Docket Number	SPLX.P0095

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No.	U.S. Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code* (if known)			
JA	1.	6,519,754	B1	02-11-2003	McElvain et al.	

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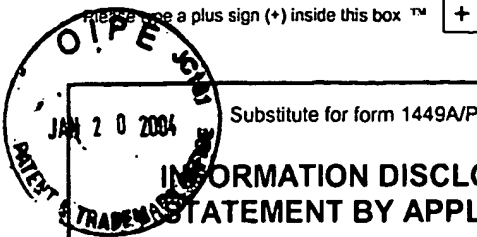
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Examiner Signature	<i>James Sun</i>	Date Considered	9-1-05
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		Number	Kind Code* (if known)			
JA	1.	2002/0157063	A1	10-24-2002	Besson	
	2.	2002/0178432	A1	11-28-2002	Kim et al.	
	3.	2003/0145288	A1	07-31-2003	Wang et al.	
	4.	4,703,435		10-27-1987	Darringer et al.	
	5.	5,003,487		03-26-1991	Drumm et al.	
	6.	5,537,330		07-16-1996	Damiano et al.	
	7.	5,892,678		04-06-1999	Tokunoh et al.	
	8.	5,903,466		05-11-1999	Beausang et al.	
	9.	5,991,524		11-23-1999	Belkhale et al.	
	10.	6,080,204		06-27-2000	Mendel	
	11.	6,311,317	B1	10-30-2001	Khoche et al.	
	12.	6,389,586	B1	05-14-2002	McElvain	
	13.	6,397,170	B1	05-28-2002	Dean et al.	
	14.	6,421,818	B1	07-16-2002	Dupenloup et al.	
	15.	6,446,240	B1	09-03-2002	Lyer et al.	
	16.	6,453,447	B1	09-17-2002	Gardner et al.	
	17.	6,470,486	B1	10-22-2002	Knapp	
	18.	6,519,609	B1	02-11-2003	Touzet	
	19.	6,539,536	B1	03-25-2003	Singh et al.	
	20.	6,543,037	B1	04-01-2003	Limqueco et al.	
JA	21.	6,546,541	B1	04-08-2003	Petranovic et al.	

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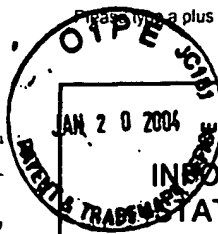
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Examiner Signature	<i>James Sun</i>	Date Considered	9-1-05
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U.S. PATENT DOCUMENTS

22.	6,618,835	B1	09-09-2003	Garlapati et al.
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NON PATENT LITERATURE DOCUMENTS

Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JSA	23.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).	
	24.	NN9411291, "Design of Portable Library using Parameterized Cells", IBM Technical Disclosure Bulletin, Vol. 37, No. 11, pp. 291-292 (4 pages).	
	25.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargeting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics, Vol. 2, 14 May 2000, pp. 703-706.	
	26.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.	
JSA	27.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.	

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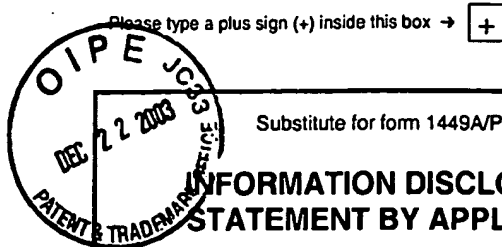
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JSA	1.	5,521,835		05-28-1996	Trimberger	
	2.	5,610,829		03-11-1997	Trimberger	
	3.	6,035,107		03-07-2000	Kuehlman et al.	
	4.	6,334,205		12-25-2001	Iyer et al.	
	5.	6,470,478	B1	10-22-2002	Bargh et al.	
	6.	6,496,972	B1	12-17-2002	Segal	
	7.	6,523,156	B2	02-18-2003	Cirit	
JSA	8.	6,574,779	B2	06-03-2003	Allen et al.	

NON PATENT LITERATURE DOCUMENTS			
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
JSA	9.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 th Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol.2, August 1997.	

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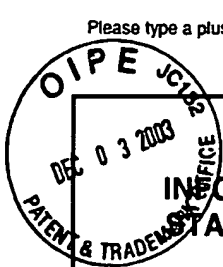
Examiner Signature	<i>James Sun & Co</i>	Date Considered	9-1-05
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Substitute for form 1449A/PTO				Application Number	10/066,188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2661 2825
				Examiner Name	LIN, SUN JAMES
Sheet	1	of	1	Attorney Docket Number	SPLX.P0095

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code* (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JSR	1.	5,519,630		05-21-1996	Nishiyama et al.	
	2.	5,537,341		07-16-1996	Rose et al.	
	3.	5,696,974		12-09-1997	Agrawal et al.	
	4.	5,574,441		05-19-1998	Tokunoh et al.	
	5.	5,787,010		07-28-1998	Schaefer et al.	
	6.	6,023,566		02-08-2000	Belkhale et al.	
JSR	7.	6,301,696	B1	11-09-2001	Lien et al.	

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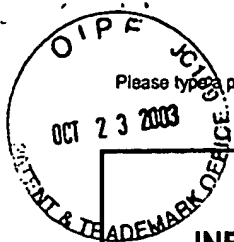
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JSR	8.	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.	
JSR	9.	Devadas, S. et al., Synthesis and Optimization for robustly delay-fault testable combinational logic circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp. 221-227.	

Examiner Signature		Date Considered	9-1-05
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/066,188
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2664 2825
				Examiner Name	LIN, SUN JAMES
Sheet	1	of	1	Attorney Docket Number	SPLX.P0095

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No.	U.S. Patent Document Number	Kind Code* (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Jed	1.	5,311,442		05-10-1994	Fukushima	
	2.	5,526,276		06-11-1996	Cox et al	
	3.	5,752,000		05-12-1998	McGeer et al	RECEIVED
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	5.	6,102,964		08-15-2000	Tse et al	Technology Center 2600
	6.	6,134,705		10-17-2000	Pedersen et al	
	7.	2001/013113		08-09-2001	Matsunaga	
	8.	6,298,472		10-02-2001	Phillips et al	
	9.	6,336,208		01-01-2002	Mohan et al	
	10.	6,473,884		10-29-2002	Ganai et al	
	11.	6,490,717		12-03-2002	Pedersen et al	
Jed	12.	6,546,539		04-08-2003	Lu et al	

Examiner Signature	<i>James Sun Lin</i>	Date Considered	9-1-05
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Substitute for form 1449A/PTO				Application Number	10/066,188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2601 2825
				Examiner Name	LIN, SUN JAMES
Sheet	1	of	2	Attorney Docket Number	SPLX.P0095

RELATED U.S. PATENT APPLICATIONS						
Examiner* • Initials	Cite No. ¹	U.S. Patent Application		Name of Patentee or Applicant of Cited Document	Date of Filing MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Serial Number				
JFA	1.	10/062,017		Steven Teig & Asmus Hetzel	01-31-02	
	2.	10/061,459		Steven Teig & Asmuz Hetzel	01-31-02	
	3.	10/062,014		Steven Teig & Asmus Hetzel	01-31-02	
	4.	10/062,044		Steven Teig & Asmuz Hetzel	01-31-02	
	5.	10/066,264		Steven Teig & Asmus Hetzel	01-31-02	
	6.	10/062,992		Steven Teig & Asmus Hetzel	01-31-02	
	7.	10/061,474		Steven Teig & Asmuz Hetzel	01-31-02	
	8.	10/061,719		Steven Teig & Asmus Hetzel	01-31-02	
	9.	10/066,456		Steven Teig & Asmus Hetzel	01-31-02	
	10.	10/062,993		Steven Teig & Asmus Hetzel	01-31-02	
JFA	11.	10/062,047		Steven Teig & Asmuz Hetzel	01-31-02	

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
JJA	12.	5,649,165		Jain et al.	07-15-97	
JJA	13.	6,301,687	B1	Jain et al.	10-09-01	

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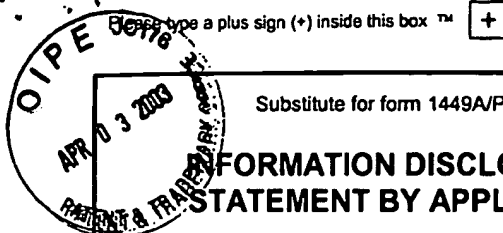
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Examiner Signature	<i>James Sun</i>	Date Considered	9-1-05
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/066,188
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2661
				Examiner Name	
Sheet	2	of	2	Attorney Docket Number	SPLX.P0095

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
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	15.	Henrik Reif Andersen, An Introduction to Binary Decision Diagrams, October 1997 (minor revisions April 1998), 36 pp.		
	16.	Jerry Burch and David Long, Efficient Boolean Function Matching, Proc. ICCAD 1992, 408-411.		
	17.	John Fishburn, A Depth-Decreasing Heuristic for Combinational Logic; or How to Convert Ripple-Carry Adder into a Carry-Lookahead Adder or Anything In-Between, Proceedings of the 27 th Design Automation Conference, 361-364, 1990.		
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	20.	Randal Bryant, Symbolic Boolean Manipulation with Ordered Binary Decision Diagrams, CMU CS Tech Report CMU-CS-92-160.		
	21.	Uwe Hinsberger and Reiner Kolla, Boolean Matching for Large Libraries, Proceedings of the 35 th Design Automation Conference, 206-211, June 1998.		
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JSA	23.	Zbigniew J. Czech, et al., An Optimal Algorithm for Generating Minimal Perfect Hashing Functions, Information Processing Letters, 43(5); 257-264, October 1992		

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